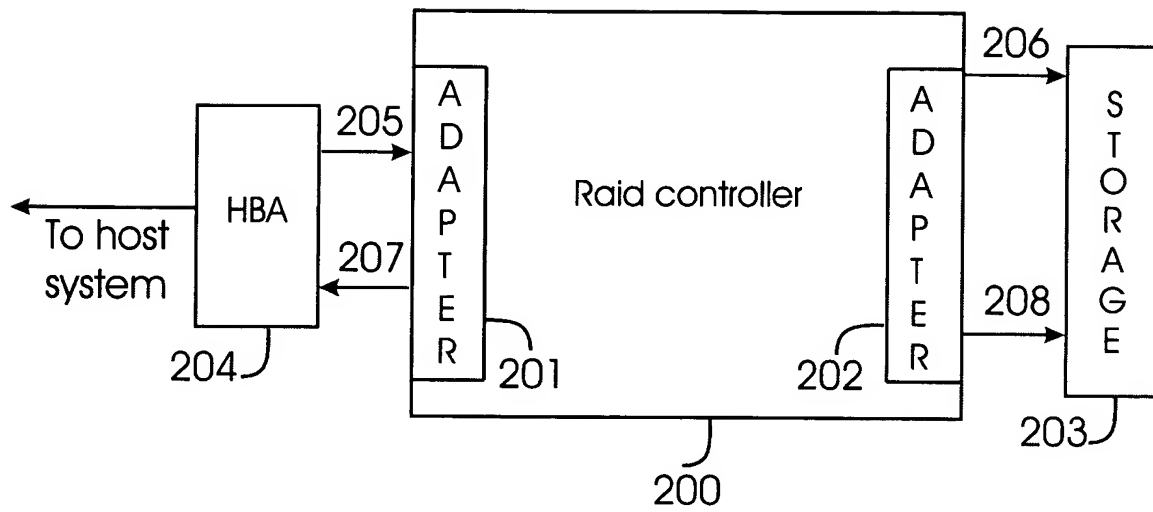


FIGURE 1



210

FIGURE 2A

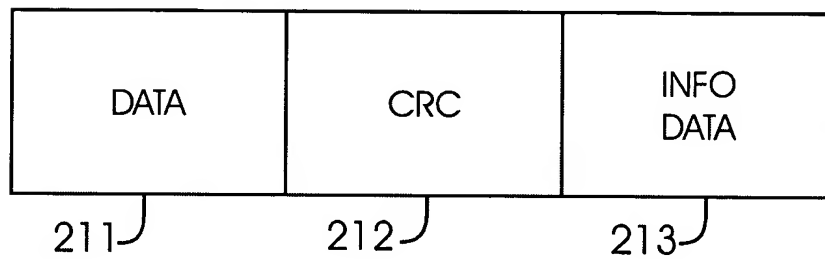
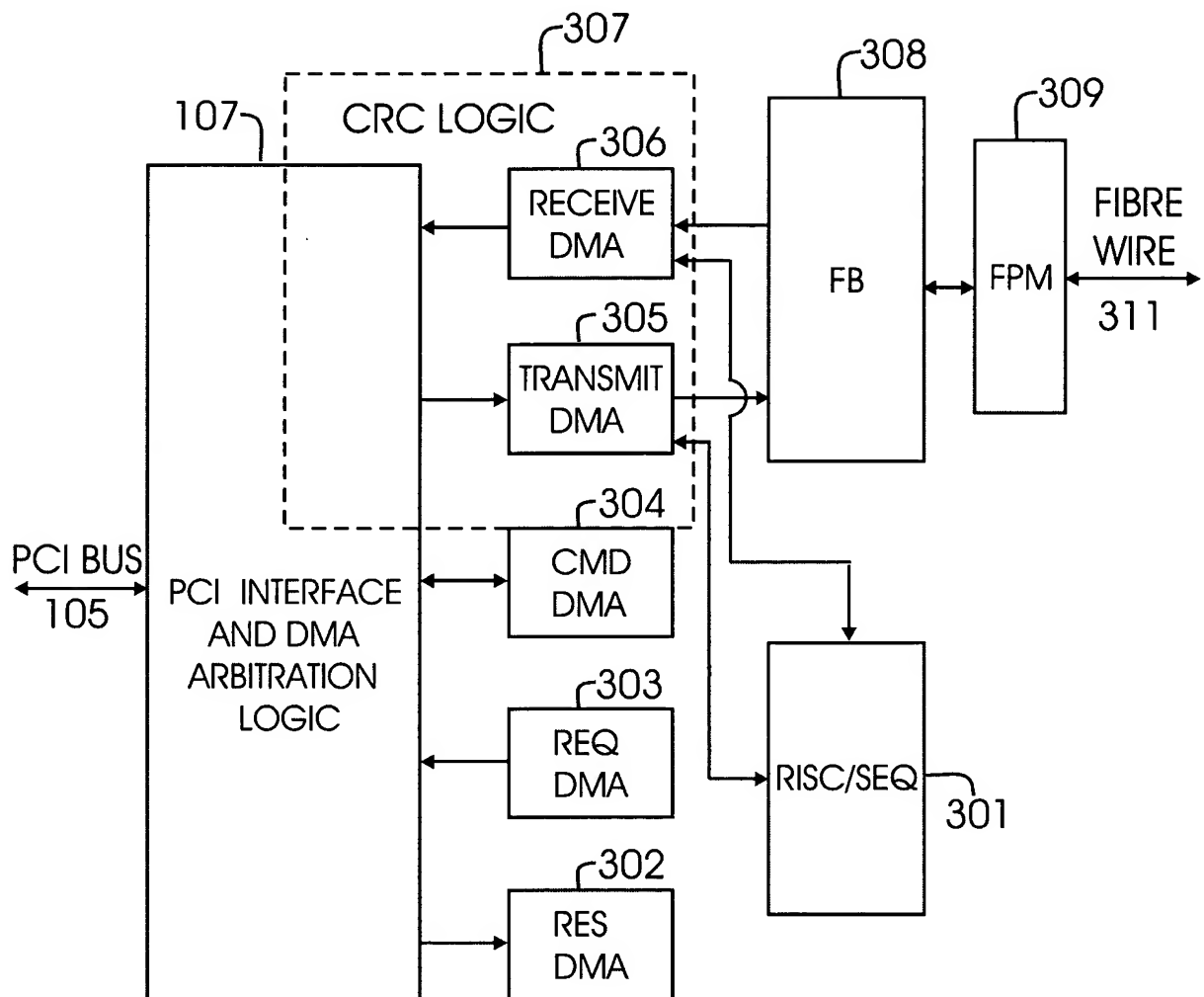


FIGURE 2B



SYSTEM BLOCK DIAGRAM

FIGURE 3

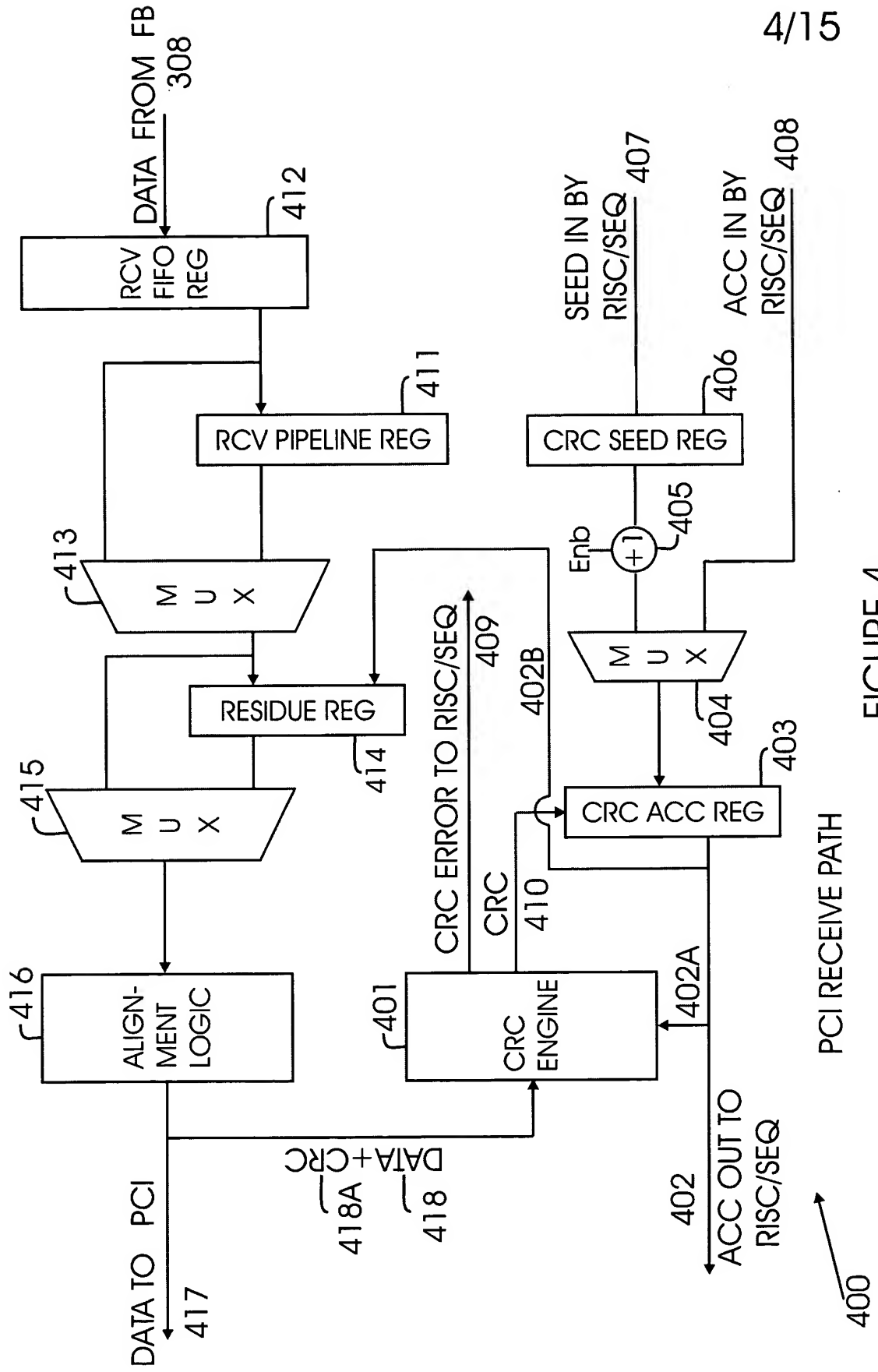


FIGURE 4

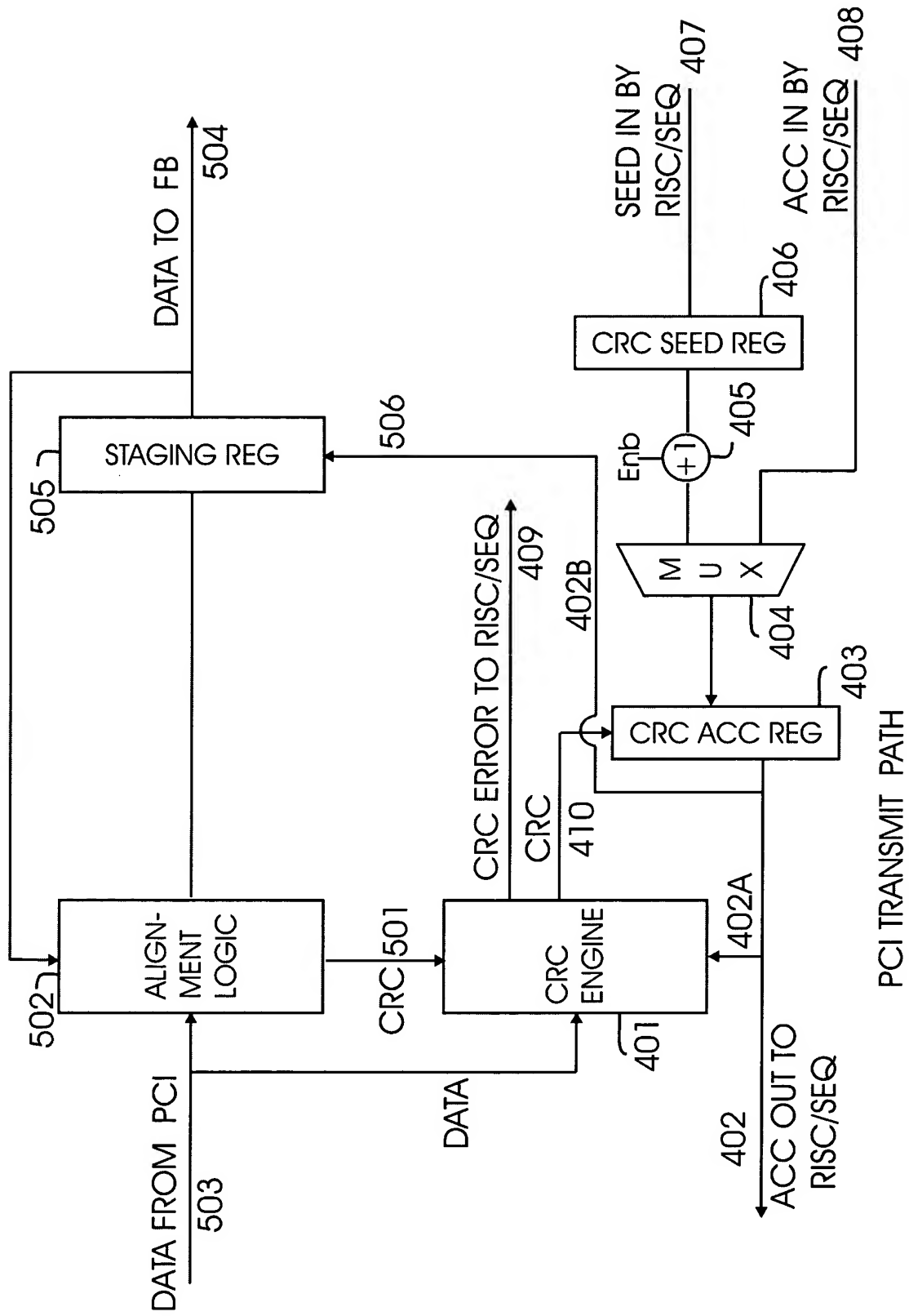


FIGURE 5

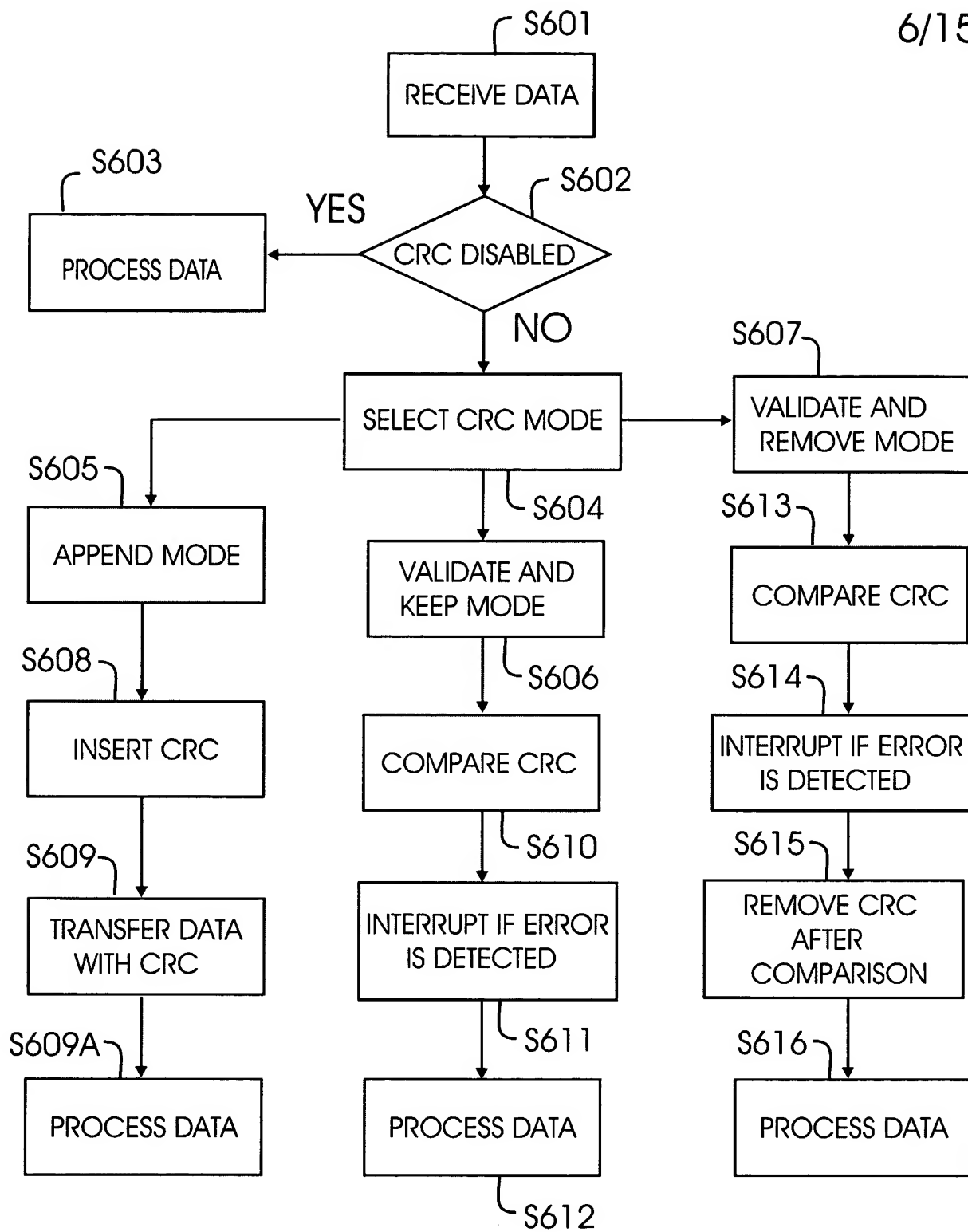


FIGURE 6

Receive DMA Register Map

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RISC Address (h)	SEQ Address (h)	Register Name	Description
320 321 322 323	20 21 22 23	RDMA Address Counter 0 RDMA Address Counter 1 RDMA Address Counter 2 RDMA Address Counter 3	These registers reflect the current PCI address. They function as a 64-bit up counter, incrementing for each byte transferred across the PCI bus. This includes the CRC protection bytes.
324 325	24 25	RDMA Transfer Counter 0 RDMA Transfer Counter 1	These registers reflect the number of bytes remaining to be transferred across the PCI bus for a segment. This includes the CRC protection bytes.
326 327	26 27	RDMA Byte Counter 0 RDMA Byte Counter 1	These registers reflect the number of bytes remaining to be transferred across the PCI bus in the total RDMA transfer. This includes the CRC protection bytes.
328 329	28 29	RDMA Relative Offset 0 RDMA Relative Offset 1	These registers reflect the number of bytes received from the RD FIFO 412. This includes the CRC bytes in Validate_And_Keep mode. This does not include the CRC bytes in Append mode.
32A	2A	RDMA Control	Bit 14 : Reserved Bit 11-10 : Reserved Bit 6 :CRC Enable Bit 5 :CRC Register Select

①

FIGURE 7A-1

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I	32B	2B	RDMA Status	II
				Bit 8 PCI Bus Error: Change in functionality. OR in Error conditions for CRC Error and Info Data Error.
	32C	2C	RDMA Frame Counter	
	32D	2D	RDMA Payload Byte Cntr	
	32E	2E	RDS Low	
	32F	2F	RDS High/ Error Enable	

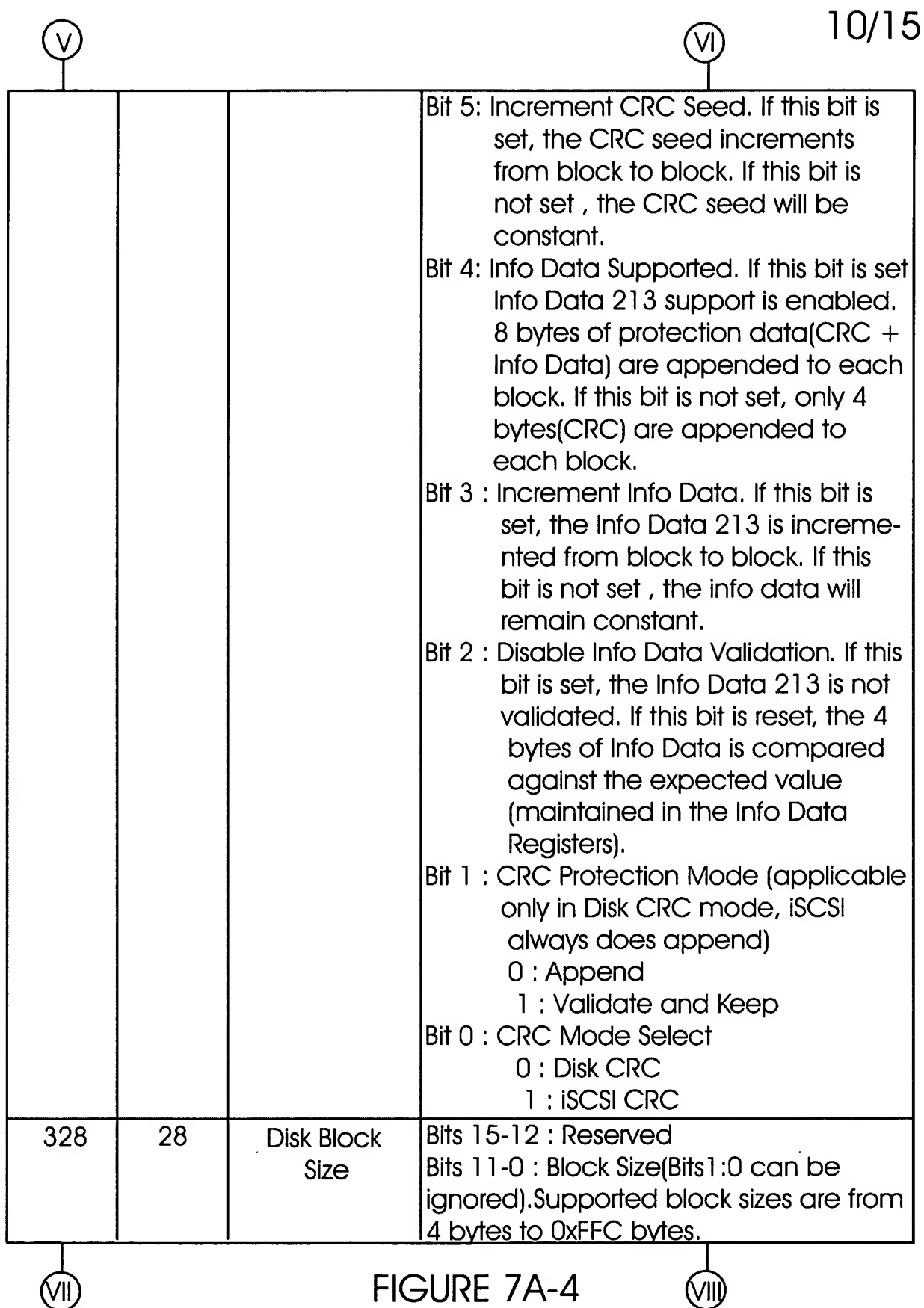
The following values are multiplexed with DMA counters and are selectable by RDMA control register bit (e.g.5 ,in this case):

320	20	RDMA CRC	The firmware writes these registers when starting a RDMA transfer. The firmware reads this register on a context switch. The value read is restored when the context resumes.
321	21	RDMA CRC Accumulator 0	
		RDMA CRC Accumulator 1	
			If the data transfer stops after CRC for Block 0 and before data for Block 1, these registers read back the CRC Seed Reload value for Block1.
			If the data transfer stops after data for Block 0 but before CRC for block 0, these registers read back CRC Value for Block 0.
322	22	CRC Seed Reload 0	These registers contain the CRC Seed Reload Value for the block being transferred.
323	23	CRC Seed Reload 1	
			If the data transfer stops after CRC for Block 0 and before data for Block 1, these registers read back CRC Seed Reload Value for Block 1.

FIGURE 7A-2

			<p>If the data transfer stops after data for Block 0 but before CRC for Block 0, these registers read back CRC Seed Reload Value for Block 1. Once data transfer for Block 0 is done, there is no need to keep seed for Block 0. The next block transfer needs seed for block 1.</p>
324	24	Block Byte Offset	<p>This register contains the number of bytes remaining for a current block (down counter), and corresponds to the CRC Accumulator registers.</p> <p>If the data transfer stops after CRC for Block 0 and before data for Block 1, this register will read back a value equal to Block Size.</p> <p>If the data transfer stops after data for Block 0 but before CRC for Block 0, this register will read back a value of ZERO.</p>
325 326	25 26	Info Data 0 Info Data 1	<p>These registers contain the Info Data 213 value for the block being transferred. If a context switch occurs on a block boundary, these registers should read back the Info Data 213 or the next block.</p>
327	27	Disk CRC Configuration	<p>This register contains the Disk CRC Configuration parameters.</p> <p>Bit 15: Select Last Block CRC Value For Read</p> <p>0 : selects accumulator for current block</p> <p>1 : selects accumulator for last block</p> <p>Bit 14:6 : Reserved</p> <p>Bit 6 : Disable CRC Validation</p>

FIGURE 7A-3



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329-32 A	29-2A	Reserved	
32B	2B	CRC STATUS	Bits 15-2 : Reserved Bits 1 : CRC Error (Validate And Keep mode only) Bits 0 : Info Data Error (Validate And Keep mode only) PCI Bus Error, bit 8 in DMA Status register is also set to 1 when any of the error status bits in CRC Status register are set.
32C-32F	2C-2F	Reserved	

FIGURE 7A-5

RISC Address	SEQ Address	Register Name	Description
90 91 92 93	20 21 22 23	TDMA Address Counter 0 TDMA Address Counter1 TDMA Address Counter 2 TDMA Address Counter 3	These registers reflect the PCI address. They function as a 64- bit up counter, incrementing for each byte transferred across the PCI bus. This includes the CRC protection bytes.
94 95	24 25	TDMA Transfer Counter 0 TDMA Transfer Counter 1	These registers reflect the number of bytes remaining to be transferred across the PCI bus for a segment. This includes the CRC protection bytes.
96	26	TDMA byte Counter 0	These registers reflect the number of bytes remaining

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FIGURE 7B-1 : TDMA Register Map

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IX

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97	27	TDMA byte Counter 1	to be transferred across the PCI bus in the total TDMA transfer. This includes the CRC protection bytes.
98 99	28 29	TDMA Relative offset 0 TDMA Relative offset 1	These registers reflect the number of bytes transferred to the TD FIFO. This includes the protection bytes in Validate_And_Keep mode. This does not include the protection bytes in Validate_And_Remove mode.
9A	2A	TDMA Control	Bit 14: Resvered Bit 11- 10: Resvered Bit 6 :CRC Enable Bit 5 :CRC Register seclect
9B	2B	TDMA Status	Bit 8 PCI Bus Error: Change in functionality. Or in Error conditions for CRC Error and Info Data Error;.
9C 9D 9E 9F	2C 2D 2E 2F	TDMA Frame Byte Counter TDMA Payload Byte Size Resvered Resvered	

The following register values are multiplexed with DMA counters and are selectable via TDMA control register bit (for example, bit 5).

90 91	20 21	TDMA CRC Accumulator 0	The firmware writes these registers when starting a TDMA tranfer.
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XI

FIGURE 7B-2

XII

XI			XII
		TDMA CRC Accumulator 1	<p>If the data transfer stops after CRC for Block 0 and before data for Block 1, these registers read back the CRC Seed Reload Value for Block 1.</p> <p>If the data transfer stops after data for Block 0 but before CRC for Block 0. These registers will read back CRC value for Block 0.</p>
92 93	22 23	CRCSeed Reload 0 CRCSeed Reload 1	<p>These registers contain the CRC Seed Reload Value for the block being transferred.</p> <p>If the data transfer stops after CRC for Block 0 and before data for Block 1, these registers read back CRC Seed Reload Value for Block 1.</p> <p>If the data transfer stops after data for Block 0 but before CRC for Block 0, these registers read back CRC Seed Reload Value for Block 0.</p>
94	24	Block byte offset	<p>This register contains the number of bytes remaining for the current block (down counter), and corresponds to the CRC Accumulator registers.</p> <p>If the data transfer stops after CRC for Block 0 and before data for Block 1, this register reads back a value equal to Block Size.</p> <p>If the data transfer stops after data for Block 0 but before CRC for Block 0, this register reads back a value of ZERO.</p>
XIII			XIV

FIGURE 7B-3

XIII			XIV
95	25	Info Data 0	These registers contain the Info Data 213 value for the block being transferred. If a context switch occurs on a block boundary, these registers should read back the Info Data for the next block.
96	26	Info Data 1	
97	27	Disk CRC configuration	<p>This register contains the Disk CRC configuration parameters.</p> <p>Bit 15: Selects last block CRC Value For Read 0: selects accumulator for current block 1: selects accumulator for last block.</p> <p>Bit 14:7: Reserved</p> <p>Bit 6: Disable CRC Validation</p> <p>Bit 5: Increment CRC seed. If this bit is set, the CRC seed increments from block to block. If this bit not set, the CRC seed will be constant.</p> <p>Bit 4: Info Data supported. If this bit is set, Info Data support is enabled. 8 bytes of protection data(CRC + Info Data) are validated on each block. If this bit not set, only 4 bytes (CRC) are validated on each block.</p> <p>Bit 3: Increment Info Data, If this bit is set, the Info Data 213 increments from block to block. If this bit is not set, the Info data will remain constant.</p> <p>Bit 2: Disable Info Data Validation. If this bit is set, the Info Data</p>
XV			XVI

FIGURE 7B-4

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XV			<p>213 is not validated. If this bit is reset, the 4 bytes of Info Data 213 are compared against the expected value (maintained in the Info Data registers).</p> <p>Bit 1 : CRC Protection Mode (applicable only in Disk CRC mode iSCSI always does Validate And Remove) 0 : Validate And Remove 1 : Validate And Keep</p> <p>Bit 0 : CRC Mode Select 0 : Disk CRC 1 : iSCSI CRC</p>
XVI			
98	28	Disk Block Size	<p>Bits 15-12 : Reserved</p> <p>Bits 11-0 : Block Size (Bits 1:0 can be ignored.) Supported Block sizes are from 4 bytes to 0xFFC byte</p>
99-9A	29-2A	Reserved	
9B	2B	CRC Status	<p>Bits 15-2 : Reserved</p> <p>Bits 1 : CRC Error</p> <p>Bits 0 : Info Data Error</p> <p>Note : PCI Bus Error, bit 8 in DMA Status register is also set to 1 when any of the error status bits in CRC Status register are set.)</p>
9C-9F	9C-9F	Reserved	

FIGURE 7B-5